I. Introduction

Recently, current mode circuits have been receiving significant attention in analog signal processing. A useful function block for high frequency current mode applications is a current conveyor. The current conveyor is a three terminal device performing many useful analog signal processing functions when the device is connected with other electronic elements in specific circuit configurations. The current conveyor has evolved from first generation to second generation. The first generation current conveyor (CCI) was proposed by Smith and Sedra in 1968 [1] and the more versatile second generation current conveyor (CCII) was introduced by the same two authors in 1970 [2], as an extension of their first generation conveyor.

In many cases, the current conveyor simplifies circuit design in much the same way as the conventional op-amp, but it presents an alternative method of implementing analog systems which traditionally has been based on op-amp. This alternative approach leads to new methods of implementing analog transfer functions, and in many cases the conveyor-based implementation offers improved performance to the voltage op-amp-based implementation in terms of accuracy, bandwidth and convenience. Circuits based on voltage op-amps are generally easy to design since the behavior of a voltage op-amp can be approximated by few simple design rules. This is also true for current conveyors. Several hundred papers have been published on the theory and applications of current conveyors. Some of these applications are shown in Fig. 1 [3, 4].

The second generation current controlled conveyor (CCCII) which implemented with the BJT and the BiCMOS technology by Fabre, etc. in 1995 [5] and 1997 [6] respectively. One of the reasons we use the CCCII is that it allows implementation of electronic functions usable at high frequency. The other reason to use the CCCII is its parasitic resistance at terminal X is controllable [7]. The controllable resistance is usable for the applications of tunable circuits, such as filters.

In order to obtain a small-size low-weight handheld system, a single-technology scheme is preferred for maximum integration level. To realize this scheme, the low-cost high-integration all-CMOS implementation is one of the most attractive solutions. Up to date, the CMOS CCCII has not yet been explored. This paper will describe the CMOS current controlled conveyor (CCCI) and its application for a tunable high frequency high Q current-mode bandpass filter [6, 8]. We will also exploit its potential in the frequency range around 200MHz~300MHz which is within the IF filter design specification of modern wireless mobile phone. The tuning of the center frequency $f_c$ and $Q$-factor can be obtained by varying two independent dc current sources.

Section II gives an overview of the current conveyor, the proposed CMOS current controlled conveyor is described in Section III, and the architecture of the second order current-mode bandpass filter is described in Section IV. Section V is the conclusion.
Fig. 1 Current conveyor applications
II. Conventional Current Conveyors

The current controlled conveyor is derived from the current conveyor. In this section, we will describe the basic idea of the CCII circuit, and the previous Bipolar implementation of CCIIs.

A. Second Generation Current Conveyor

The block diagram of a second generation current conveyor (CCII) is shown in Fig. 2. The CCII has three terminals X, Y, and Z. The relationship of terminal currents and voltages is defined as [2]:

\[
\begin{pmatrix}
i_y \\
v_x \\
i_z
\end{pmatrix}
= \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \Box & 1 & 0 \end{pmatrix}
\begin{pmatrix}
v_y \\
i_x \\
v_z
\end{pmatrix}
\]

(1)

The above equation indicates: voltage \( v_x \) follows voltage \( v_y \), currents \( i_z \) follows current \( i_x \), and the current \( i_y \) is equal to zero. The zero current indicates terminal Y has an infinite input resistance. By convention, the positive current indicates the current flow into the device. The \( \Box \) sign indicates the \( i_x \) and \( i_z \) are in the same direction or opposite.

According to Eq. (1), we know that an ideal CCII is a combination of a voltage follower and a current follower. The voltage follower is between terminal Y and terminal X, and the current follower is between terminal X and terminal Z. A simplified representation of CCII is shown in Fig. 3. An ideal voltage follower has infinite input impedance and zero output impedance, and an ideal current follower has zero input impedance and infinite output impedance.
Fig. 3 Simplified representation of CCII
B. CCII in Practice

Nevertheless, a practical implementation of the CCII can never be ideal. The input resistance $Z_y$ at terminal Y and the output resistance $Z_z$ at terminal Z may not be infinite, the input resistance $Z_x$ at terminal X may not be zero, and the voltage gain and current gain may not be unity. In order to optimize the design for high-frequency operation, it is necessary to consider a more realistic model for the CCII. In Fig. 4, a widely used equivalent circuit is shown to describe the conveyor analytically at high frequency [6, 9, 10].

![Fig. 4 High-frequency model for the CCII](image)
C. Translinear Implementation of CCII+

The circuit, shown in Fig. 5 [11], uses a mixed translinear cell between terminal Y and X, which is biased by $I_o$. Output Z, which duplicates the current flowing through terminal X, is realized in a conventional manner, using two complementary mirrors.

The input cell, with mixed translinear loop, contains two PNP and two NPN transistors. It is characterized by the translinear relationship between collector currents of these transistors [11]:

$$I_{c1}I_{c3} = I_{c2}I_{c4} \tag{2}$$

The circuit is biased by dc current $I_o$ ($I_{c1} = I_{c3} \equiv I_o$, by assuming current gain $\beta$ of the transistors much greater than unity). Thus, it presents a high impedance input terminal Y and a low impedance output terminal X. This cell acts as a voltage follower. The voltage difference between terminals X and Y depends on the value of the current $i_x(t)$; its expression is given by

$$V_{XY}(t) = -V_T \log \frac{I_{c2}(t)}{I_o} \tag{3}$$

where $V_T \equiv kT/q \equiv 26mV$ at 27°C is the thermal voltage. The relationship Eq. (2) allows, in the particular case of the loop shown in Fig. 5 (i.e., for $I_{c1} = I_{c3} \equiv I_o$), to calculate the expressions for the currents $I_{c2}(t)$ and $I_{c4}(t)$. They are given by [11]

$$I_{c2}(t) = \frac{1}{2} \left[ \left( i_x^2(t) + 4I_0^2 \right)^{1/2} - i_x(t) \right] \tag{4}$$

$$I_{c4}(t) = \frac{1}{2} \left[ \left( i_x^2(t) + 4I_0^2 \right)^{1/2} + i_x(t) \right] \tag{5}$$

Now, with the assumption, $|i_x(t)| \ll 2|I_o|$, Eq. (3) and Eq. (4) lead to

$$V_{XY}(t) = \frac{V_T}{2I_o} i_x(t) \tag{6}$$

The relationship shows that the output small signal resistance of the equivalent voltage follower is

$$R_x = \frac{V_T}{2I_o} \tag{7}$$

So, $R_x$ can be controlled by varying the bias current $I_o$ of the loop.
Fig. 5 Translinear implementation of CCII+
D. Previous Current Controlled Conveyors

The schematic of the CCCII+ deduced from Fig.5 implemented by BJT [5, 12] and BiCMOS [6, 8] are shown in Fig. 6. Two current mirrors (transistor $Q_5$ to $Q_7$ and $Q_{10}$, $Q_{11}$) allow the translinear loop to be biased by the current $I_o$. Note that the MOS transistors in Fig. 6(b) are used for the biasing to minimize noise, the main contribution in noise coming from the current mirrors.

In this paper, we will show that it is possible to take advantage of this parasitic resistance on terminal X of CCCII because its value depends on the bias current of the conveyor. Thus the CCCIIIs allow current conveyor applications to be extended to the domain of electronically adjustable functions.

From Eq. (7), $R_x$ can be controlled by $I_o$. This property can be applied for some useful applications [12] such as: (1) controllable voltage-current conversion (see Fig. 7), (2) negative current controlled resistance (Fig. 8), and they are used in our design of a bandpass filter.

1) Controllable voltage-current conversion

When the terminal Y of the CCCII+ is grounded and terminal X constitutes the input of the circuit, the output current $I_z(t) = i_z(t)$ is then given by

$$I_{out}(t) = \frac{1}{R_x} V_{in}(t)$$

(8)

Its value is therefore controllable by the bias current $I_o$. The input resistance of this circuit, seen from terminal X is equal to $R_x$.

2) Negative current controlled resistance

The circuit represented in Fig. 8 simulates a grounded negative resistance which value: $Z_{in} = -R_x$ is current controlled, and we will discuss it in Section IV-C.
Fig. 6 The schematic implementation of CCCII+ (a) BJT, (b) BiCMOS
Fig. 7 Voltage-current conversion with Y grounded

\[ i_x(t) = \frac{V_{in}(t)}{Z_o} \]

\[ i_z(t) = I_{out} \]

Fig. 8 Negative current controlled resistance
III. CMOS Current Controlled Conveyor

In this section we will describe our design of a CMOS current controlled conveyor and show the simulation results.

A. Circuit Description and Analysis

The circuit shown in Fig. 9(a) is similar to the translinear implementation of the CCCII+ shown in Fig. 6. The input cell, M1-M4, contains two N-MOS and two P-MOS transistors, and the voltage at terminal X follows the voltage supplied at terminal Y. The transistors M5-M11 form a controllable bias circuit. Two complementary current mirrors M12-M13, M14-M15 make the current flowing through terminal Z duplicates the current flowing through the terminal X. The transistors M16-M17 and M18-M19 improve the input impedance $R_x$ and output impedance $R_y$, respectively. Fig. 9(b) presents the equivalent model of the current conveyor giving the input and output impedance of each terminal, and Fig. 9(c) shows the equivalent circuit between terminal Y and X.

Since the input impedance $Z_x$ is strongly related to the performance of the bandpass filter, it is studied in detail here. Referring to the Fig. 9(a), the expression of $R_x$ is given by the following formula [13]:

$$R_x = \frac{1}{g_{m2} + g_{m4}}$$  \hspace{1cm} (9)

where $g_m$ is the MOSFET transconductance controlled by $v_{gs}$. For a MOS transistor, it can be shown that the transconductance are proportional to $\sqrt{I_o}$, so that the input resistance $R_x$ depends on the bias current.

Assume P-MOS and N-MOS transistors are matched. Including all the parasitics in terminal X, the input impedance $Z_x$ is

$$Z_x = \frac{1}{2} \frac{s(C_{gsv1} + C_{gsv2}) + g_{m1}}{(sC_{gsv1} + g_{m1})(sC_{gsv2} + g_{m2})}$$  \hspace{1cm} (10)

Fig. 9(d) shows the detailed equivalent circuit.
Fig. 9 CMOS current controlled conveyor (CCCII+) (a) Schematic implementation, (b) Equivalent model of the CCCII+
Fig. 9 CMOS current controlled conveyor (CCCII+) (c) Equivalent circuit between Y and X, (d) Practical circuit of terminal X including parasitic elements
Expressions of $R_{ax}$ and $R_{ab}$ are

$$R_{ax} = \frac{1}{2} g_{m2} \left( C_{gs1} + C_{gs2} \right)^2 - \left( g_{m1} C_{gs2} + g_{m2} C_{gs1} \right) \left( C_{gs1} + C_{gs2} \right) + C_{gs1} C_{gs2} g_{m1}$$

$$R_{ab} = \frac{1}{2} \left( g_{m1} C_{gs2} + g_{m2} C_{gs1} \right) \left( C_{gs1} + C_{gs2} \right) - g_{m1} C_{gs1} C_{gs2}$$

and $R_x = R_{ax} // R_{ab} = 1/2 g_{m2}$. The expression of the input inductance is

$$L_x = \frac{1}{2} \frac{C_{gs1} + C_{gs2}}{g_{m1}} R_{ax}$$

and the parasitic capacitor $C_x$ is

$$C_x = 2 \frac{C_{gs1} C_{gs2}}{C_{gs1} + C_{gs2}}$$

**B. Simulation Results**

In this design, the bias current $I_0$ is equal to 100µA using ±2.5V power supply voltages, and Table I gives the transistor design parameters. Fig. 10 shows the voltage transfer characteristic $A_v$ ($=v_x/v_y$) with an open circuit node X and a grounded node Z. The 3dB cutoff frequency is 950MHz, and the voltage gain at low frequency is around 0.973. Fig. 10 also shows the current transfer characteristic $A_i$ ($=i_x/i_y$) when nodes Y and Z are grounded. Its 3dB bandwidth is about 380MHz, and the gain of the current transfer is 0.927. The simulated impedance $Z_x$ is shown in Fig. 11. The calculated value of parasitic elements ($R_{ax} = 2.25K \Omega$, $R_{ab} = 445 \Omega$, $L_x = 0.66 \mu H$, and $C_x = 0.18pF$) are very approximate to the simulated curve. Table II gives the simulation results.

Table III shows the comparison of the BJT [12], BiCMOS [8] and CMOS implementations. In this table, $I_0$ is equal to 50µA and supply voltages are ±2.5V.
### TABLE I
TRANSISTOR DESIGN PARAMETERS

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M17</td>
<td>100/0.5</td>
</tr>
<tr>
<td>M3, M4, M12, M13</td>
<td>45/0.55</td>
</tr>
<tr>
<td>M5, M6</td>
<td>15/0.5</td>
</tr>
<tr>
<td>M7</td>
<td>16.5/0.5</td>
</tr>
<tr>
<td>M8, M9</td>
<td>45/0.5</td>
</tr>
<tr>
<td>M10</td>
<td>75/0.55</td>
</tr>
<tr>
<td>M11</td>
<td>90/0.55</td>
</tr>
<tr>
<td>M14, M15, M19</td>
<td>10/0.5</td>
</tr>
<tr>
<td>M16, M18</td>
<td>25/0.55</td>
</tr>
</tbody>
</table>

### TABLE II
BASIC CHARACTERISTICS OF THE CCCII+ (CMOS),
\( I_0 = 100 \, \text{µA}, \quad \pm 2.5\text{V SUPPLY VOLTAGE} \)

<table>
<thead>
<tr>
<th></th>
<th>Voltage follower</th>
<th>Current follower</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>0.973</td>
<td>0.927</td>
</tr>
<tr>
<td>-3dB Bandwidth</td>
<td>950MHz</td>
<td>380MHz</td>
</tr>
<tr>
<td>Input impedance</td>
<td>78KΩ//0.28pF</td>
<td>371Ω</td>
</tr>
<tr>
<td>Output impedance</td>
<td>371Ω</td>
<td>591KΩ//0.14pF</td>
</tr>
<tr>
<td>Offset current at Y</td>
<td>1.24 µA</td>
<td>1.24 µA</td>
</tr>
<tr>
<td>Output offset</td>
<td>5.5mV</td>
<td>2.19 µA</td>
</tr>
</tbody>
</table>

15
**TABLE III**  
**BASIC CHARACTERISTICS OF THE CCCII+**  
$I_0 = 50 \, \mu A, \pm 2.5V$ **SUPPLY VOLTAGE**

<table>
<thead>
<tr>
<th></th>
<th>BJT</th>
<th>BiCMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage follower</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>0.9984</td>
<td>0.996</td>
<td>0.974</td>
</tr>
<tr>
<td>-3dB bandwidth</td>
<td>1.1GHz</td>
<td>1.5GHz</td>
<td>628MHz</td>
</tr>
<tr>
<td>Input impedance</td>
<td>323KΩ//0.54pF</td>
<td>72KΩ//0.55pF</td>
<td>132KΩ//0.22pF</td>
</tr>
<tr>
<td>Output impedance</td>
<td>263Ω</td>
<td>228Ω</td>
<td>567Ω</td>
</tr>
<tr>
<td>Offset current at Y</td>
<td>2.1µA</td>
<td>89µV</td>
<td>2.9µA</td>
</tr>
<tr>
<td>Output offset</td>
<td>32µV</td>
<td>89µV</td>
<td>5.5mV</td>
</tr>
<tr>
<td><strong>Current follower</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>1.022</td>
<td>1.022</td>
<td>0.974</td>
</tr>
<tr>
<td>-3dB bandwidth</td>
<td>615MHz</td>
<td>680MHz</td>
<td>290MHz</td>
</tr>
<tr>
<td>Input impedance</td>
<td>263.8Ω</td>
<td>228Ω</td>
<td>567Ω</td>
</tr>
<tr>
<td>Output impedance</td>
<td>319.6Ω//0.5pF</td>
<td>276KΩ//0.5pF</td>
<td>900KΩ//0.15pF</td>
</tr>
<tr>
<td>Output offset</td>
<td>3.4µA</td>
<td>3.9µA</td>
<td>2.2µA</td>
</tr>
</tbody>
</table>
Fig. 10 Voltage transfer ($v_x/v_y$) characteristics, when node X is opened and node Z is grounded, and Current transfer ($i_x/i_y$) characteristics, when nodes Y and Z are grounded. \( I_0 = 100 \mu A, V^+ = -V^- = 2.5V, V_a = -V_b = 0.5V, V_c = V_d = 0V \)

Fig. 11 The simulated and calculated X-input impedance when \( I_0 = 100 \mu A, V^+ = -V^- = 2.5V, V_a = -V_b = 0.5V, V_c = V_d = 0V \)
Since the circuit is current controlled, we are interested in the characteristics by varying the value of the controlled current $I_o$. **Fig. 12** presents the variation of the intrinsic $Z_x$ (see **Fig. 9(d)**) as a function of the dc bias current $I_o$. **Fig. 13** gives the values $R_x$ obtained from SPICE simulations with the CCCII+, as well as the theoretical ones calculated from Eq. (9). As shown, the simulated values of the controlled resistance are in good agreement with theoretical ones. Deviations less then 10% were obtained in the range 10µA~500µA for $I_o$. The most important deviation, which appear either for the very low or very high values of $I_o$ principally come from the difference that exist between $I_o$ and the current of transistors M1 and M3. These current deviations result from the current gains of transistors operating for very high or very low values of currents. When the bias current $I_o$ is less then 10µA, the deviation is more then 10%; and when $I_o$ is more then 500µA, the variation of parasitic resistance $R_x$ is not evident, so the range of the controlled current is defined from 10µA~500µA in practice. Simulation results show that its value is tunable from 172Ω to 1.65KΩ.

The variation of voltage gain and current gain under the bias current $I_o$ can be seen in **Fig. 14**. On the range from 10µA~500µA, the gain of voltage follower and current follower are about unity. **Fig. 15** presents the 3dB cutoff frequency of the voltage follower and current follower, obtained by varying $I_o$. The bandwidth of $A_v$ and $A_i$ can be up to 2.1GHz and 640MHz respectively when $I_o = 500µA$. 
(a) \[ R_{ba} (\Omega) \]

Bias current \( I_o \) (\( \mu A \))

(b) \[ R_{vb} (\Omega) \]

Bias current \( I_o \) (\( \mu A \))
Fig. 12 The variation of the intrinsic $Z_x$ as a function of the dc bias current $I_0$. 
Fig. 13 Theoretical and simulated values for $R_s (=R_{sa}\parallel R_{sb})$
Fig. 14 The variation of voltage gain and current gain under the bias current $I_o$

Fig. 15 The 3dB bandwidth of voltage follower and current follower, obtained by varying $I_o$
IV. Second Order Bandpass Filter

The basic idea of a tunable bandpass filter is derived from a parallel \( RLC \) resonant circuit, which resonant frequency and \( Q \)-factor can be tuned by a variable inductance and a variable resistance. The variable inductance is implemented with two CCCII+s, and a controlled negative impedance converter (NIC) in parallel with the \( RLC \) circuit makes the resistance tunable.

A. Parallel \( RLC \) Resonant Circuit

The typically parallel \( RLC \) tank circuit is shown in Fig.16. Its resonant frequency is

\[
\omega_0 = \frac{1}{\sqrt{LC}} \tag{15}
\]

and the quality factor \( Q \) of the parallel \( RLC \) network is:

\[
Q = \frac{R}{\omega_0 L} = \omega_0 RC = R \sqrt{\frac{C}{L}} \tag{16}
\]

From Eq. (15) and Eq. (16), if the inductance is variable the \( \omega_0 \) can be tuned; and also if the resistance is variable the \( Q \) can be tuned.

The tunable inductance \( L \) is implemented with two CCCII+s connected as a gyrator, and the tunable resistance is implemented with a CCCII+ connected as a negative impedance converter (NIC). These will be described in the following sections.

Fig. 16 Parallel \( RLC \) tank circuit
B. Current-Controlled Active Inductance

Consider the circuit connection shown in Fig. 17(a), where the CCII+s are ideal. The equivalent circuit derived from this connection is shown in Fig. 17(b), where the equivalent inductance $L_{eq}$ is

$$L_{eq} = R_{s1} R_{s2} C_1$$

(17)

The input resistances of practical CCII+s can take the place of the external resistances, and these resistances are controllable as practical CCII+s are replaced by the CCCII+s. The circuit is shown in Fig. 17(c) [6, 8].

Fig. 17 Nonideal inductance: (a) Implementation from two CCII+ and two external resistances (b) Electrical equivalent impedance
Fig. 17 Nonideal inductance: (c) Implementation of the controlled inductance by using the intrinsic parasitic resistance at terminal X of CCCII+
C. Negative Impedance Converter

The parallel resistances $R_s$ in Fig. 17(b) usually reduce the $Q$-factor. In order to increase the $Q$-factor, we need to increase the resistance $R$ in Fig. 16. A simple way to increase $R$ is using negative resistance in parallel with $R_s$, The negative resistance can be implemented with a CCCII+ connected as Fig. 18 [6, 8, 12].

To cancel the effect of the parasitic shunt resistors, a negative resistor in parallel with the inductance is needed. The practical current conveyor can be configured in such a way to perform the function of the negative impedance converter (NIC), which is useful for implementation of the filter. The circuit represented in Fig. 18 simulates a grounded negative resistance which value: $Z_{in} = -R_s$ is current controlled. Since the current through the input node is $i_z + i_y = i_z = i_x$, and $v_x = v_y$, the input impedance $Z_{in} = v_x / (i_x) = -R_s$, that the circuit in Fig. 18 is a NIC.

![Negative Resistor Implemented from CCCII+](image-url)
D. CCCII+ Bandpass Filter Design

1. Circuit Description and Analysis

Fig. 19 shows the current mode second-order elementary bandpass filter [6, 8]. The first and second CCCII+ and capacitor \( C_1 \) implement the inductance as previously described. The third acts as a controlled negative resistance, as indicated in Fig. 20. Finally, the fourth CCCII+ constitutes an output current source. The transfer function of the filter is given by [8]

\[
\frac{I_{out}(s)}{I_{in}} = \frac{\left[ \frac{R_{x1} R_{x2} C_1}{R_{x4}} \right] s}{1 + \left[ \frac{R_{x1} R_{x2} C_1}{R_{eq}} \right] s + \left( \frac{R_{x1} R_{x2} C_1 C_2}{R_{x3}} \right) s^2}
\]

(18)

and

\[
\frac{1}{R_{eq}} = \left[ \frac{1}{R_{x1}} + \frac{1}{R_{x2}} + \frac{1}{R_{x4}} - \frac{1}{R_{x3}} \right]
\]

(19)

Its characteristic parameters are the following:

\[
\Omega_0 = \frac{1}{\sqrt{R_{x1} R_{x2} C_1 C_2}}
\]

(20)

\[
Q = \frac{R_{eq}}{\sqrt{R_{x1} R_{x2} C_1 C_2}}
\]

(21)

2. \( f_o \) Tuning

From Eq. (20) and Eq. (21) it is obvious that one can modify the center frequency \( f_o \) and the \( Q\)-factor independently of each other, the way to tune the center frequency of the filter is to vary the value of \( R_{x1} \) and \( R_{x2} \). Referring to Eq. (20), an appropriate choice to simplify the tuning of \( f_o \) is to use the same current \( I_{o1} \) for \( I_{o1} \) and \( I_{o2} \). Then it follows that \( R_{x1} = R_{x2} \), and we can modify \( f_o \) by varying this current \( I_{o} \) keeping the other currents (\( I_{o3} \) and \( I_{o4} \)) fixed.
3. $Q$ Tuning

From Eq. (19) and Eq. (21) we can see that $Q$ can be tuned either from $I_{o3}$ or $I_{o4}$ (see Fig. 19) without affecting the value of $f_o$ and with a theoretical possibility of making $Q$ infinite if $R_{eq}$ in Eq. (19) tends to infinite. For example, let the first, second and forth conveyors have the same bias current $I_o$ (i.e., $R_{o1} = R_{o2} = R_{o4} = R_x$), when the input impedance of the third conveyor (NIC) is $R_{o3} = -R_x/3$, the $Q$ is theoretically infinite. Thus when the bias current $I_o$ and $I_{o4}$ are fixed, the $Q$-factor can be modified just only by varying the current $I_{o3}$.

![Fig. 19 Second order bandpass filter operating in current-mode](image)
E. Practical Inductance, NIC and Bandpass Filter

However, the parasitic effects which cannot be ignored will influence the theoretical values. The parasitics at node X are more complex (see Section III and Fig. 9(d)), and there is a parasitic resistance \( R_p = R_x // R_y \) in parallel with \( C_1 \), also there is an additional resistance \( r_p = (R_x R_y) / R_p \) appears in series with \( L_{eq} \). When all the parasitics of the controlled conveyors (i.e., parasitic impedance: \( R_x // C_y \), \( R_y // C_z \), and nonideal values of the voltage and current transfer \( A_y \) and \( A_z \)) are taken into account, rearrange the above equations, we can get that [6]

\[
L_{eq} = R_x R_y C_1 / A_y A_z
\]

\[
r_p = (R_x R_y) / A_y A_z R_p
\]

The detail equivalent circuit for this controlled inductance is shown in Fig. 20(a). Note that the input impedance \( Z_{in} \) of the NIC shown in Fig. 18 is now replace \( -R_x \) with \( -A_y A_z / Zx \), and the transfer functions of the practical bandpass filter are [6]

\[
\frac{I_{out}(s)}{I_{in}} = \frac{s \left( \frac{R_x R_y C_1}{A_y A_z} \right)}{1 + \left( \frac{R_x R_y C_1}{A_y A_z R_{eq}} \right) s + \left( \frac{R_x R_y C_1 C_2}{A_y A_z} \right) s^2}
\]

where

\[
R_{un} = R_{un} // R_{shn}
\]

\[
\frac{1}{R_{eq}} = \frac{1}{R_x} + \frac{1}{R_y} + \frac{1}{R_x} - \frac{A_y A_z}{R_x}
\]

\[
C_1 = C_{z1} + C_{y2}
\]

\[
C_2 = C_2 + C_{y3} + C_{z3}
\]
Their characteristic parameters are given as

\[ \Omega_0 = \sqrt{\frac{A_x A_i}{R_{x1} R_{x2} C_1 C_2}} \]  

(29)

\[ Q = \sqrt{\frac{A_x A_i}{R_{x1} R_{x2}}} \frac{R_{eq}}{\sqrt{C_1 C_2}} \]  

(30)

The equivalent circuit of controlled inductance may be simplified as shown in Fig. 20(b) because \((R_{xu} + sL_x) \ll \left(\frac{R_{sb}}{sC_x}\right)\) when operating in high frequency. The voltage gain \((A_x)\) and current gain \((A_i)\) approximate to unity at low frequency, the value of capacitor \(C_2 \equiv C_2'\) and \(r_p \ll sL_{eq}\) when the circuit is operated at high frequency. See from the bandpass filter’s input, this filter is now equivalent to a shunt \(RLC\) circuit as shown in Fig.21 where \(C_x' = C_x + C_{x1} + C_{x2} + C_{x4} - C_{x3}\) and \(R_x = R_{sb1} // R_{sb2} // R_{sb4}\).

\[ L_{eq} \leq \frac{R_{xu}}{2} \]

\[ r_p \leq \frac{L_x}{2} \]

\[ 2C_x \leq \frac{R_{sb}}{2} \]

(a)

(b)

Fig. 20 Parasitical current-controlled active inductance (a) It’s detail equivalent circuit, (b) The simplified circuit when operating in high frequency
Fig. 21 The input impedance see from the bandpass filter’s input
F. Simulation Results

Fig. 22(a) shows the value of this simulated inductance, using the CCCII+ with 100µA bias current and ±2.5V voltage sources. The circuit in Fig. 17(c) was designed with $I_{o1} = I_{o2} = 100$µA, and the following parameters are extracted from the design: $C_1 = 0.42$pf, $R_{x1,2} = 2.25$KΩ, $R_{ob1,2} = 445$Ω, the parasitic inductance $L_{x1,2} = 0.66$µH, and the parasitic capacitor $C_{x1,2} = 0.18$pf. Fig. 22(b) compares the impedance variation of this circuit (Fig. 17(c)) in parallel with the value of $(-Z_x/2)$, and the theoretical impedance $(r_p + sL_{eq})$. We can see a good agreement between both curves. The values of $L_{eq}$ and $r_p$ extracted from the simulations: 0.9µH and 2.1Ω were found in good accordance with theoretical ones (0.92µH and 3.2Ω, respectively) from Eq. (22) and Eq. (23).

The capacitor $C_2$ is always 2.3pf in our tunable bandpass filter design. Fig. 23 shows the tunability of the center frequency with the bias current $I_o$ (from Eq. (29) and Eq. (30)). In this figure, we vary the current $I_o$ (50µA, 100µA, and 200µA) with $I_{o3} = I_{o4} = 350$ µA. The higher the bias current $I_o$, the higher the center frequency $f_o$. Fig. 24 shows the tunability of the $Q$-factor with the current $I_{o3}$ (Eq. (26) and Eq. (30)). The controlled current $I_{o3}$ is varier as 300µA, 330µA, 350µA, and 360µA with $I_o = I_{o4} = 100$ µA. From this simulation, it can be seen that $Q$-tuning is very sensitive. Even with a small change of $I_{o3}$, the $Q$-factor changes largely. Besides, we find that not only the $Q$-factor but also $f_o$ is tuned. This is because the parasitic capacitors in parallel with $C_2$ which influence the center frequency (see Eq. (28)) are also changed.

Fig. 25 indicates that this configuration is quite useful for an IF bandpass filter which center frequency is from 200MHz to 300MHz which is within the IF design specification of modern wireless mobile phone. The $Q$-factor in this configuration is up to 800. Table IV lists the comparison among the tunable bandpass filter implemented with BiCMOS [8] and CMOS.

<table>
<thead>
<tr>
<th></th>
<th>BiCMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_o$</td>
<td>30 MHz ~ 120MHz</td>
<td>55 MHz ~ 410MHz</td>
</tr>
<tr>
<td>Q</td>
<td>1 ~ 140</td>
<td>1~800</td>
</tr>
</tbody>
</table>
Fig. 22 Parasitical current-controlled active inductance (a) The simulated inductance (b) Frequency variation of $\left( Z_\text{in} \left( \frac{-Z_x}{2} \right) \right)$ and $(r_p + sL_{\text{eq}})$
Fig. 23 Second-order bandpass filter: frequency tuning. $I_{o3} = I_{o4} = 350\mu A$ and $C_2 = 2.3\text{pF}$. $I_o = 50\mu A, 100\mu A, \text{ and } 200\mu A$.

Fig. 24 Second order bandpass filter: $Q$ tuning. $I_{o3} = 300\mu A, 330\mu A, 350\mu A \text{ and } 360\mu A$, $I_o = I_{o4} = 100\mu A$ and $C_2 = 2.3\text{pF}$.
V. Conclusion

The CMOS CCCII and the tunable bandpass IF filter based on the CCCII are successfully developed. Simulations show that they are suitable for the application around 200MHz~300MHz which is the specification of current wireless mobile phone.
References


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